

REMARKS

The specification has been amended to correct typographical errors and to more clearly explain the purpose of the application. Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly solicited.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By 

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Attachments

(Rev. 12/19/01)

10029145.122801

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph beginning on page 7, line 3 has been amended as follows:

[31] In another aspect of the present invention, a pad structure of an LCD device includes a substrate, a metal film formed on the substrate, and [a]an amorphous transparent conductive film formed on the metal film.

The paragraph abridging pages 8 and 9 has been amended as follows:

As shown in FIG. 3A, a material for forming a gate line (100) is deposited on a glass substrate 11 as a single film of Cu or [CU/TI]CU/Ti, or as a deposition film sequentially formed of Cu and Cu/Ti by using sputtering or other techniques. Then, photolithography is performed to form the gate line, a gate electrode 12a and a gate pad 12b. A gate insulating film 13 made of a silicon nitride film, silicon oxide film, etc. is formed on the entire surface of the glass substrate 11 including the gate electrode 12a and the gate pad 12b. Although the glass substrate 11 is preferred as a substrate, the substrate may be formed with other materials.

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The paragraph beginning on page 10, line 19, has been amended as follows:

FIG. 4A to FIG. 4D are sectional views showing manufacturing process steps of the LCD device according to the embodiment of the present invention, taken along lines [IV-IV]III-III' (TFT region) and V-V' (data pad region) of FIG. 3.

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